Call for Participation

THE 3RD INTERNATIONAL TEST CONFERENCE IN ASIA, 2019

Tokyo Senju Campus, Tokyo Denki University, TOKYO, JAPAN
September 3-5, 2019.

http://www.itc-asia.info.hiroshima-cu.ac.jp/2019/

ITC-Asia (International Test Conference in Asia) is the Asian regional version of ITC (International Test Conference) which has been held in the United States. ITC has been a flagship conference on test technology of computer systems and semiconductor integrated circuits since 1970. ITC / ITC-Asia aims not only to publish the results of academic research, but also as a place for presenting leading-edge technologies in the industry, as well as for academic and industrial interaction. With an attempt to stimulate more discussion around the globe, the 1st ITC-Asia was initiated in Taipei in 2017, and the 2nd ITC-Asia was held with great success in Harbin China in 2018.

In 2019, the 3rd ITC-Asia will take place in Tokyo Senju Campus of Tokyo Denki University in Tokyo Japan, on Sept. 3-5. This year, we have organized 2 Tutorials, 2 Keynote Speeches, 3 Invited Talks, 10 Technical sessions, 2 Special Sessions, 1 Embedded Tutorial, 2 Industry Sessions, and Two days Exhibition. We would like to invite all interested Researchers, Engineers, Technologists, and Students to participate in ITC-Asia 2019.

Program Highlights

Tutorials:

◆Machine Learning for Reliability of ICs and Systems
-Mehdi Tahoori (Karlsruhe Institute of Technology),
-Krishnendu Chakrabarty (Duke University)

◆AI Chip Technologies and Its DFT Methodologies
-Yu Huang, Rahul Singhal and Lee Harrison
(Mentor, A Siemens Business)

Invited Talks:

◆IC Test – Where the Excitement Never Ceases to End
-Rohit Kapu (Cadence Design Systems, Inc.)

◆Semiconductor Device and Test in Data Explosion Period
-Shin Kimura (ADVANTEST CORPORATION)

◆Implementation of Security Function utilizing Safety Verification Function for Collaboration of Security and Safety
-Nobuyasu Kanekawa (Hitachi, Ltd.)

Special Sessions:

◆The New High-Bandwidth Test Access Paradigm
-Steve Pateras (Synopsys, Inc.)

◆Test Challenges and Solutions for AI, SoC DFT Architecture and Next Level of Quality
-Yang, Wu (Mentor, a Siemens Business)

◆High Quality and Low Cost Test for Mixed Signal SOCs
-Malav Shah (Texas Instruments, Inc)

◆*ITC-India Excellent Papers*

Keynote Speeches:

◆Highly Dependable Many-Processor Systems-on-Chip for Cars
-Hans G. Kerkhoff (University of Twente)

◆AI-Baseball: Semiconductor, IOT, and the Sport Industry
-Cheng-Wen Wu (National Tsing Hua University)

Technical Sessions: 30 papers

◆Analog and Mixed-signal Test,
◆ATE Design, Trust & Safety,
◆Hardware Oriented Security,
◆DFT, ATPG, Fault Tolerance,
◆Hotspot Analysis/Yield Analysis,
◆3D IC Test/ SRAM BIST, Delay Test

Industry Sessions:

◆FormFactor Inc.
◆Syswave Corp.
◆ADVANTEST CORPORATION
◆Renesas Electronics Corporation

Exhibitors:

◆Synopsys, Inc.
◆Mentor, a Siemens Business
◆Cadence Design Systems, Inc.
◆ADVANTEST CORPORATION
◆Syswave Corp.
◆ABLIC Inc.
◆Renesas Electronics Corporation

Platinum Partners

Gold Partner

Silver Partner

Registration

You can register for participation via http://www.itc-asia.info.hiroshima-cu.ac.jp/2019/attendance/registration or by scanning the QR code

Early Registration Deadline: July 30, 2019

For further information, please visit our Home Page

http://www.itc-asia.info.hiroshima-cu.ac.jp/2019/

Or contact:

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Sponsors: