



The 4<sup>th</sup> IEEE Int'l Test Conference in Asia, 2020

# (IEEE ITC-Asia 2020)

September 22-25, 2020

CO-LOCATED with SEMICON Taiwan

Taipei, Taiwan

Web site: <http://sscas.ee.ncku.edu.tw/ITC-Asia-2020/HOME.html>



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## Call For Papers

(Outstanding papers with extension will be invited to ITC'20)

With the test technology facing its grand challenges to ensure the quality, safety, and security of today's ICs and electronic systems incorporating more and more sophisticated manufacturing processes and system integration technologies in various emerging applications such as Internet of Things, cloud computing, automotive electronics, etc., global proliferation and cooperation has grown increasingly even more important. International Test Conference has been a flagship conference in test technology since 1970. With an attempt to stimulate more discussion and interaction between the academia and the industry around the globe, ITC-Asia was initiated as a sister conf. of ITC in 2017. This year, it is again co-located with SEMICON Taiwan in Taipei city. Welcome to join us to immerse ourselves in not only the state-of-the-art test technology, but also numerous semiconductor industry forums organized by SEMICON Taiwan.

Topics of Interests include (but are not limited to) the following topics:

- Design Validation and Debug
- Hardware Oriented Security and Thrust
- ATE Design
- Analog and Mixed-Signal Test
- RF Test
- High-Speed I/O Test
- Fault Modeling and Simulation
- ATPG (Automatic Test Pattern Generation)
- Design for Testability for Logic Circuits
- Built-In Self-Test for Logic Circuits
- Delay Test
- System-on-Chip Test
- Test Compression
- Test Methods for Low-Power Circuits
- Power-Aware and/or Thermal-Aware Test
- Memory Test, Diagnosis, and Repair
- Fault Diagnosis and Failure Analysis
- Test Methods for Emerging Devices
- MEMS Test
- Sensor Test
- CPU/GPU Test
- Automotive IC Test
- Test Methods for Internet of Things
- Online Test
- On-Chip Measurement
- Reliability Issues
- SiP, 2.5D, and 3D IC Test
- Interconnect Test
- Test Standards
- Test Economics
- Fault Tolerance
- Reconfigurable System Test
- Board-Level Testing and Diagnosis
- Yield Analysis and Learning

**Submission:** (Check out the [conference web site](#) for the entry)

Regular paper submissions should be made electronically by PDF manuscripts only, not exceeding 6 pages in IEEE 2-column format (including abstract, figures, tables, and bibliography). A submission will be considered evidence that upon acceptance at least one author will attend the conference to make the presentation. Authors of accepted papers are also responsible for preparing the final manuscripts in time to be included in the electronic proceedings, which will eventually be published in *IEEE Xplore* Digital Library. At least one full registration to the conference is required for each accepted paper.

### Key Dates

- **Submission of title and abstract:** Feb. 16, 2020
- **Paper submission:** Feb. 23, 2020
- **Notification of acceptance:** April 26, 2020
- **Camera-ready manuscript:** June 7, 2020



National Cheng Kung University



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