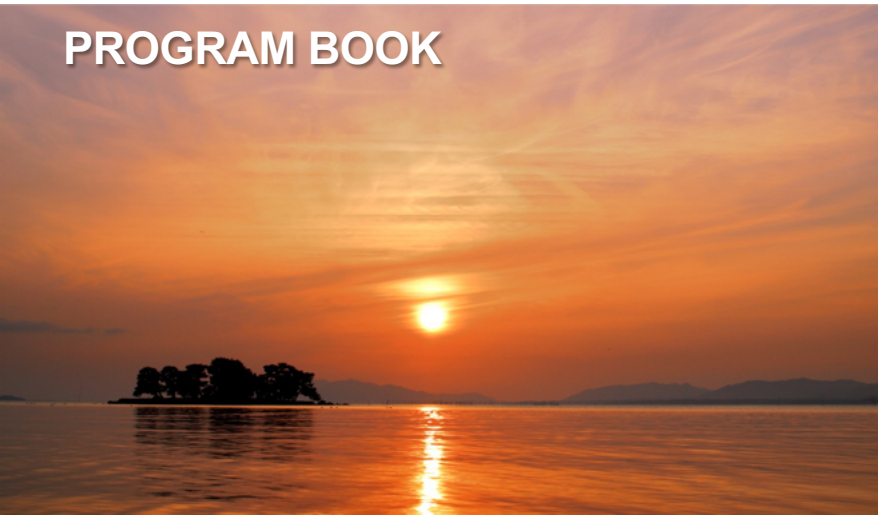
THE 7TH IEEE INTERNATIONAL TEST CONFERENCE IN ASIA (ITC-ASIA) 2023

Kunibiki Messe, Matsue, Shimane, Japan
September 12–14, 2023

PROGRAM BOOK



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Foreword

Welcome to the 7th International Test Conference in Asia (ITC-Asia 2023)!

International Test Conference (ITC) organized by IEEE has long been the world's premier conference dedicated to the electronic testing technologies - covering the complete cycle from design, verification, manufacturing, test and diagnosis, reliability, and failure analysis. In order to lead the electronic testing community in Asia, ITC-Asia was launched for the first time in Taipei in 2017.

This year the 7th ITC-Asia will be held in Matsue, Shimane prefecture in Japan, on Sept. 12–14 with discussion and interaction between the academia and the industry around the globe. Through attractive sessions on the state-of-the-art test technology trend and the industry topics, attendee can confront challenges faced by the industry, and learn how these challenges are being addressed by the combined efforts of academia, tool and equipment suppliers, designers, and test engineers.

ITC-Asia 2023 received 31 research paper submissions from nine countries and regions. Each paper was sent to at least three reviewers for evaluation, and 13 regular papers and seven short papers were selected based on the reviewers' rating and comments. The selected papers were allocated into seven technical sessions. In addition to the technical sessions, we have further enriched the contents of the conference with the arrangement of two half-day tutorials, two keynote speeches, two invited talks, two 3D chiplet test sessions, three special/industry sessions, five industrial exhibitions, and several high-school student presentations. We would like to thank the Organizing Committee and the Program Committee of ITC-Asia 2023 for their delight hard work in managing all aspects of the conference. Our heartfelt thanks to the ITC-Asia Steering Committee for help for their cooperation.

Finally, we would like to thank our speakers and organizers for their significant contributions to ITC-Asia 2023 and thank the program participants to make the conference successful. We hope that all participants enjoy the conference and the technical discussions.

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General Information

Venue Location

Kunibiki Messe (Shimane Prefectural Convention Center)

Conference Date

Day 1: 9:00 am – 4:00 pm, Sept. 12, Tuesday, 2023

Day 2: 8:40 am – 9:00 pm, Sept. 13, Wednesday, 2023

Day 3: 9:00 am – 4:00 pm, Sept. 14, Thursday, 2023

Registration Desk

The registration desk will be located in front of the International Conference Hall on the 3rd floor of Kunibiki Messe. It will be open during the following hours:

Sept. 12, Tue. 8:30 am – 6:00 pm

Sept. 13, Wed. 8:10 am – 4:00 pm

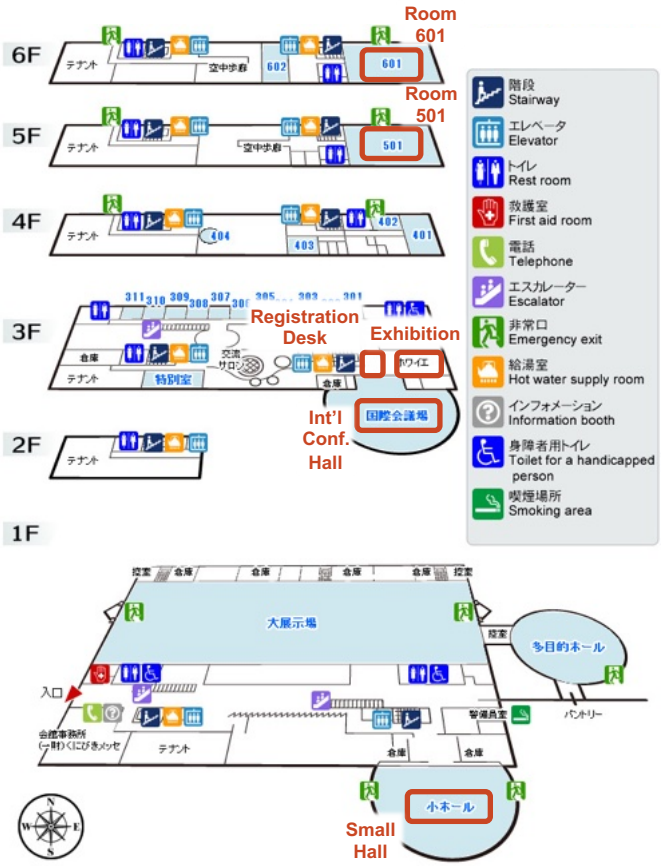
Sept. 14, Thu. 8:30 am – 4:00 pm

Please print your name tag (emailed to you) before you come to the registration desk.

Lunch

Lunch will be provided to all attendees on Sept. 13 and Sept. 14. The place for lunch/coffee break is located at the Small Hall in the 1st floor (ground floor) of Kunibiki Messe.

Venue Floor Plan



◆ **Int'l Conf. Hall (3rd floor):**
Tutorials, Opening, Keynotes, Invited Talks, Sessions 1A, 2A, 3A and 4A
(Registration Desk / Industry Exhibition in front of the hall)

◆ **Room 501 (5th floor): Sessions 1B, 2B, 3B and 4B**

◆ **Room 601 (6th floor): Sessions 1C, 2C, 3C and 4C**

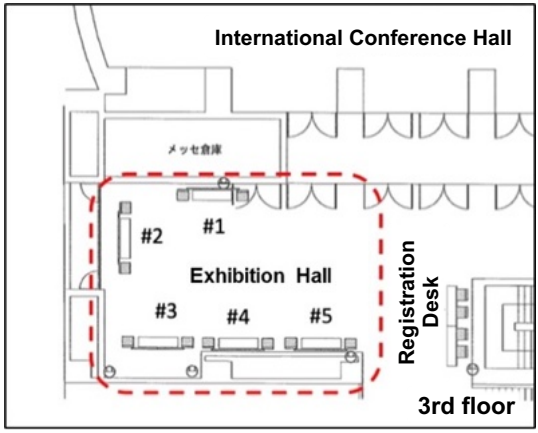
◆ **Small Hall (1st floor): Coffee/Lunch Break, Poster Presentations**

Exhibition & Poster

Industry Exhibition

Period: Sept. 13, Wed., 8:00 am – Sept. 14, Thu., 3:00 pm

Location: Exhibition Hall in front of Int'l Conf. Hall



#1: TAKAYA, #2: Siemens EDA, #3: S.E.R., #4: Cadence, #5: FormFactor

Exhibitors:

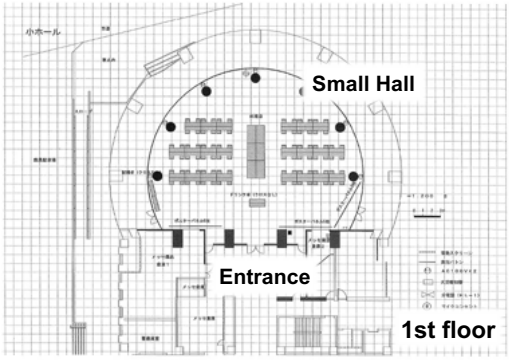
summaries

- ◆ Cadence Design Systems, Inc. (#4)
- ◆ FormFactor Inc. (#5)
- ◆ S.E.R Corporation (#3)
- ◆ Siemens EDA (#2)
- ◆ TAKAYA Corporation (#1)

Poster Presentations by High School Students

Period: Sept. 14, Thu., 11:00 am – 1:00 pm

Location: Small Hall



Social Program: Banquet

Our banquet will be held at Restaurant “紅葉(Momiji, Red Leaves)” of Yuushien Garden, where you can enjoy a traditional Japanese-style garden, on Sept. 13, from 6:30 pm to 9:00 pm. During the banquet, you can also enjoy Yasugibushi, which is a famous folk song in the Yasugi region, Shimane Prefecture.

The conference registration fee for IEEE Member and Non-member includes a banquet fee. You will find a banquet ticket in your name holder.

Our charter bus transferring from the conference venue to Yuushien and back to the JR Matsue Station is organized. The bus will depart from the conference venue to Yuushien at 5:30 pm, and back to the station at 9:00 pm.

We hope you enjoy our social program!

Yuushien Garden

Yasugibushi

Overall Agenda

		Int'l Conf. Hall	Room 501	Room 601	
Sept.12 (Tue.)	9:00 am – 12:00 pm	**Tutorial 1 @Int'l Conf. Hall** Scalable hierarchical DFT technologies for AI, SOC and multi-die Lee Harrison and Wu Yang (Siemens EDA)			
	1:00 pm – 4:00 pm	**Tutorial 2 @Int'l Conf. Hall** Silicon Lifecycle Management: Trends, Challenges and Solutions Yervant Zorian (Synopsys, Inc.)			
		Int'l Conf. Hall	**Room 501**	**Room 601**	
Sept. 13 (Wed.)	8:40 am – 10:50 am	**Opening @Int'l Conf. Hall**			**Industry Exhibition @Exhibition Hall in front of Int'l Conf. Hall (flexibly opened during 8:00 am – 4:00 pm)**
		Keynote 1 @Int'l Conf. Hall Semiconductor Packaging Revolution in the Era of Chiplets Yasumitsu Orii (Rapidus Corporation)			
		Invited Talk 1 @Int'l Conf. Hall Moore Meets Murphy Erik Jan Marinissen (imec)			
	10:50 am – 1:00 pm	*Lunch Break* ***@Small Hall***			
	1:00 pm – 2:15 pm	**Regular 1A:** Hardware Security	**Special 1B:** 3D Chiplet Test Session 1	**Special 1C:** Siemens Session (Silicon Lifecycle Management)	
	2:15 pm – 2:45 pm	*Coffee Break* ***@Small Hall***			
	2:45 pm – 4:00 pm	**Regular 2A:** Defect Analysis	**Special 2B:** 3D Chiplet Test Session 2	**Special 2C:** Industry Session 1	
	5:30 pm – 9:00 pm	**Social Program: Banquet @Yuushien Garden**			
		Int'l Conf. Hall	**Room 501**	**Room 601**	
Sept. 14 (Thu.)	9:00 am – 10:50 am	**Keynote 2 @Int'l Conf. Hall** Technology for The Future of Computing Shintaro Yamamichi (IBM Japan, Ltd.)			**Industry Exhibition @Exhibition Hall in front of Int'l Conf. Hall (flexibly opened during 8:00 am – 3:00 pm)**
		Invited Talk 2 @Int'l Conf. Hall Test Industry Challenges and Solutions as Observed by the Leading Physical Implementation Solution Provider Janet Olson (Cadence Design Systems, Inc.)			
	10:50 am – 1:00 pm	*Lunch Break* / ***Poster Presentations by High School Students @Small Hall***			
	1:00 pm – 2:15 pm	**Regular 3A:** Processor/Software Testing	**Regular 3B:** Fault Tolerant Latch	**Special 3C:** Industry Session 2	
	2:15 pm – 2:45 pm	*Coffee Break* ***@Small Hall***			
	2:45 pm – 4:00 pm	**Regular 4A:** Testing and Verification	**Regular 4B:** Memory	**Regular 4C:** Jitter and Error Mitigation	

: Tutorials
: Opening, Keynotes, Invited Talks
: Regular Sessions
: Exhibition & Poster
: Social Program
: Special/Industry Sessions

Tutorials

Tutorial 1

9:00 am – 12:00 pm, Sept. 12 Tue., @Int'l Conf. Hall

Scalable hierarchical DFT technologies for AI, SOC and multi-die

Lee Harrison and Wu Yang (Siemens EDA)

Abstract:

In this tutorial, we will proceed to give an overview of the exciting field of AI and HPC. It will cover the critical and special characteristics and the architecture of the popular AI chips. Next, we will summarize the features of the AI chips from design-for-test (DFT) perspective and introduce the DFT technologies that can help testing AI chips. Similarly, we will the discussion on DFT for typical HPC SOC designs. We will also look at how the shift to 2.5D and 3D including Chiplet development is changing the industry, the new challenges added for the DFT community and the solutions. Finally, we will present a few case studies on how DFT is implemented in the real AI chips. We will also present some of the functional monitoring techniques that are available today. An overall architecture showing how functional monitoring can be implemented and how the monitor data can be used to manage in-life capabilities.

About the Lecturers:

Lee Harrison, is Tessent Product Marketing Director for safety and security, at Siemens EDA. He has over 20 years of industry experience with Siemens Tessent test, safety and security products, with a focus on automotive, Lee is working to ensure that current and future test, safety, security and analytics requirements of Siemens's automotive customers are understood and met. Lee received his BEng in Micro Electronic Engineering from Brunel University London in 1996.

Wu Yang is the Director of marketing at Siemens EDA. With more than 24 years of experiences in DFT, 3D IC, silicon learning and testing, Mr. Yang has been a frequent speaker at many conferences and a regular contributor to papers and articles. He delivered multiple tutorials at ITC, ATS, ETS and VTS. Mr. Yang received a MS degree in electrical engineering from Portland State University.

Tutorials

Tutorial 2

1:00 pm – 4:00 pm, Sept. 12 Tue., @Int'l Conf. Hall

Silicon Lifecycle Management: Trends, Challenges and Solutions

Yervant Zorian (Synopsys, Inc.)

Abstract:

Recent advances in automotive SOCs, artificial intelligence accelerators, and high-performance computing engines in data centers have led to an explosion in the adoption of emerging technology nodes and 3DIC/chiplet packages. This tutorial will present today's trends and discuss on the resiliency challenges for such emerging SOCs. It will then focus on optimizing the SOC health using advanced solutions typically utilized for managing the different silicon lifecycle stages: from silicon debug in early bring up stage to shorten the time-to-volume; to self-test and repair during volume production stage, in order to improve quality and yield; to power-on self-test in the field stage to address aging challenges; to periodic checking in-system to improve functional safety; and finally to fault tolerance and error correction during mission mode to address a range of transient errors. All of the above optimizations are materialized by on-chip and/or off-chip data analytics.

About the Lecturer:

Dr. Yervant Zorian is a Chief Architect and Fellow at Synopsys, as well as President of Synopsys Armenia. Formerly, he was Vice President and Chief Scientist of Virage Logic, Chief Technologist at LogicVision, and a Distinguished Member of Technical Staff AT&T Bell Laboratories. He is currently the President of IEEE Test Technology Technical Council (TTTC), the founder and chair of the IEEE 1500 Standardization Working Group, the Editor-in-Chief Emeritus of the IEEE Design and Test of Computers and an Adjunct Professor at University of British Columbia. He served on the Board of Governors of Computer Society and CEDA, was the Vice President of IEEE Computer Society, and the General Chair of the 50th Design Automation Conference (DAC) and several other symposia and workshops.

Dr. Zorian holds 35 US patents, has authored four books, published over 350 refereed papers and received numerous best paper awards. A Fellow of the IEEE since 1999, Dr. Zorian was the 2005 recipient of the prestigious Industrial Pioneer Award for his contribution to BIST, and the 2006 recipient of the IEEE Hans Karlsson Award for diplomacy. He received the IEEE Distinguished Services Award for leading the TTTC, the IEEE Meritorious Award for outstanding contributions to EDA, and in 2014, the Republic of Armenia's National Medal of Science.

He received an MS degree in Computer Engineering from University of Southern California, a PhD in Electrical Engineering from McGill University, and an MBA from Wharton School of Business, University of Pennsylvania.

Keynotes

Keynote 1

9:00 am – 9:50 am, Sept. 13 Wed., @Int'l Conf. Hall

Chair: Masahiro Ishida (ADVANTEST CORPORATION)

Semiconductor Packaging Revolution in the Era of Chiplets

Yasumitsu Orii (Rapidus Corporation)

Abstract:

Since the semiconductor cost for state-of-the-art nodes is increasing, "Chiplet" technology is in the spotlight as a new evolutionary path to scale up integration and improve performance and reduce the total cost. With an SoC, a chip might incorporate a CPU, plus an additional several IP blocks on the same chip. That design is then scaled by the advanced node, which is an expensive process. With a chiplet model, those several IP blocks are hardened into smaller dies(chiplets) and those dies are integrated on an interposer to build a system. Those chips must be connected in the shortest length while considering signal integrity and power integrity so that the cutting-edge packaging technology is the key to improve the performance of IT equipments. In this presentation, the advanced 2.1D, 2.3D, 2.5D and 3D packaging technologies will be introduced as well as the several interposer technologies.

About the Speaker:

Dr. Yasumitsu Orii joined IBM Japan in 1986 and was a leading expert on Flip Chip organic packages, which had contributed to the performance improvements and miniaturization of such products as servers, laptop computers, and HDDs. The packaging technology is becoming more important for next generation server products as Moore's Law reaches its limits. His flip chip expertise extended into many related areas. Initially, he was a pioneer of flip chip on FPC (Flexible Printed Circuit) for HDDs, which allowed the read/write amplifier ICs to be mounted on the suspension and much closer to the GMR head. Later, he developed the C2 (Chip Connection) technology that supported low-cost 50-μm-pitch flip chip bonding for the commodity consumer electronics market and it was licensed to a company in Taiwan. At IBM Research Tokyo, he was leading the next generation flip chip organic package, 3D-IC projects and Neuromorphic Computing for IBM Servers and creating new technologies under a Joint Development Program involving many leading Japanese materials companies. He left IBM in 2014 and joined NAGASE & CO., LTD.

Keynotes

He established “New Value Creation Office” under the direct control of the president and launched the material informatics software as a service in 2020. He left NAGASE and he joined Rapidus Corporation in 2022/Dec. Now he is the senior managing executive officer to lead the 3D Assembly Division. He is IMAPS(International Microelectronics Assembly and Packaging Society) Fellow, IEEE EPS(Electronics Packaging Society) Senior member.

Keynotes

Keynote 2

9:00 am – 9:50 am, Sept. 14 Thu., @Int'l Conf. Hall

Chair: Hideyuki Ichihara (Hiroshima City University)

Technology for The Future of Computing

Shintaro Yamamichi (IBM Japan, Ltd.)

Abstract:

We are now facing a dramatical transformation in the IT industry, especially computing technologies. A new generation of the transistors, having a gate-all-around and nanosheet structure, is developed. In parallel, new semiconductor chips dedicated for the AI workload have been intensively studied. One technology, called Digital Core, can save the energy by reducing the precision in the calculation. The other technology, called Analog Core, utilizes non-volatile memory elements to represent the weights of the neural network in an analog way, and performs the multiply and accumulate operation by physical mechanism. Since it is quite difficult to implement all these technologies and architectures in one die, the advanced packaging technology, including testing methodology, will play a critical role in terms of system integration. Especially in a small form factor, such as in interposer substrate scale, the "chiplet" platform with both technology and design aspects should be developed, and recognized in the semiconductor ecosystem. Several chiplet technologies, such as micro bumping and Si bridge interconnect, will be introduced.

About the Speaker:

Shintaro Yamamichi received his M.E. and Ph. D. degrees in electrical engineering, from Kyoto University, Japan in 1989 and 2002, respectively. He was involved in both semiconductor and packaging process research in NEC and Renesas Electronics. He was also a visiting industrial fellow at University of California, Berkeley in 1997. In 2013, he joined the Science and Technology team in IBM Research -Tokyo. From 2016, He led the research projects, including quantum computer installation, AI hardware, advanced packaging and material informatics. Currently, he is the Director of Semiconductors, IBM Research -Tokyo, leading all the semiconductor-related research and development activities in IBM Japan.

Invited Talks

Invited Talk 1

10:00 am – 10:50 am, Sept. 13 Wed., @Int'l Conf. Hall

Chair: Masayuki Arai (Nihon University)

Moore Meets Murphy

Erik Jan Marinissen (imec)

Abstract:

Gordon Moore's iconic 1965 article unwittingly laid the foundation for a remarkably accurate prediction that has withstood the test of time. His forecast has turned into an industry target, holding immense significance. For decades, downsizing metal and poly pitches effortlessly propelled progress, but now the technical and economical limits of this scaling approach are in sight. Today, the semiconductor industry seeks salvation in the vertical dimension through die stacking, commonly referred to as "chiplet-based design". However, even these multi-die packages, like all integrated circuits, are susceptible to Murphy's Law and necessitate rigorous testing for manufacturing defects. Beyond the usual obstacles of test content, accessibility, and cost, chiplet-based ICs present their own unique set of test challenges. This presentation aims to scrutinize these hurdles and explore emerging solutions, if available.

About the Speaker:

Erik Jan Marinissen is Scientific Director at imec in Leuven, Belgium, where he is responsible for research on test and design-for-test, covering topics as diverse as 3D-stacked ICs, silicon photonics, CMOS technology nodes below 10nm, and STT-MRAMs. In addition, he holds the position of Visiting Researcher at Eindhoven University of Technology (TU/e) in the Netherlands. Previously, he worked at NXP Semiconductors and Philips Research Laboratories in Eindhoven, Nijmegen, and Sunnyvale. He holds an MSc degree in Computing Science (1990) and a PDEng degree in Software Technology (1992) from TU/e. Marinissen has an extensive publication record, co-authoring more than 285 journal and conference papers and being involved in the invention of eighteen US/EP patent families.

Invited Talks

Marinissen has played significant roles in standardization and academic initiatives. He served as Editor-in-Chief of IEEE Std 1500™-2005, which focuses on embedded core test access, and initiated and chaired IEEE Std 1838™-2019, addressing 3D test access. Additionally, he founded workshops such as 'Diagnostic Services in Network-on-Chips', '3D Integration Workshop', and the IEEE 'International Workshop on Testing Three-Dimensional Stacked ICs'. Marinissen has also taken on key positions as Program Chair and General Chair for several conferences, including DDECS, ETS, 3D-TEST, 3DC-TEST, DATE, ETW, DSNOC, and 3DIW. Moreover, he serves on various conference committees, contributing to events such as ATS, DATE, ETS, ITC, ITC-Asia, and VTS. Marinissen serves on the editorial boards of IEEE 'Design & Test' and Springer's 'Journal of Electronic Testing: Theory and Applications'. Throughout his career, Marinissen has received numerous prestigious awards, including Best Paper Awards at various conferences and symposiums. Both in 2008 and 2010, he won the Most Significant Paper Awards at the IEEE International Test Conference (ITC). In 2017, he received both the National Instruments' Engineering Impact Award and the IEEE Standards Association's Emerging Technology Award. At ITC 2021, Marinissen received the TTTC Bob Madge Innovation Award. Notably, he was recognized as the most-cited author of ITC papers from 1995 to 2019 on ITC's 50th anniversary in 2019. He is also included in the list of "Top-2% Scientists World-Wide in All Disciplines" published by Elsevier and Stanford University. Marinissen is a Fellow of IEEE, a Distinguished Contributor Charter Member, and a Golden Core Member of IEEE Computer Society. He served as an elected member of the IEEE Computer Society's Board of Governors from 2019 to 2021. Marinissen has also shared his expertise through tutorials and in-house company courses on Core-Based SOC Test, 3D-SIC Test, and Improving ATPG Test Quality at various international conferences and events.

As an educator, Marinissen has supervised over 49 international MSc and PhD students, fostering their growth and development in the field. Notably, Dan Adolfsson, one of his MSc students from Linköping Universitet in Sweden, received the "Sveriges Ingenjörer 'Lilla Polhempriset'" in 2007 for his outstanding MSc graduation project supervised by Marinissen at NXP Semiconductors. Furthermore, Lizhou Wu, a PhD student at TU Delft in the Netherlands, was honored with the TTTC Edward J. McCluskey Best Doctoral Thesis Award in Test at ITC in 2021 for his exceptional PhD thesis titled "Testing STT-MRAM: Manufacturing Defects, Fault Models, and Test Solutions", which received a "cum laude" distinction.

Invited Talks

Invited Talk 2

10:00 am – 10:50 am, Sept. 14 Thu., @Int'l Conf. Hall

Chair: Satoshi Komatsu (Tokyo Denki University)

Test Industry Challenges and Solutions as Observed by the Leading Physical Implementation Solution Provider

Janet Olson (Cadence Design Systems, Inc.)

Abstract:

Test is a mission critical aspect of the design process, but design functionality/verification consumes the significant majority of engineering focus, with test often retrofitted late in the design cycle. The era of point-tools is over, what's needed is deep collaboration across the flow from state-of-the-art design IP, verification, physical design, and packaging. New solutions must manage test structures from multiple sources and meet coverage, test time, and PPA (power, performance, area) goals without introducing design closure iterations. This presentation offers a new way forward, borne from Cadence's unique perspective gained from experience working with global semiconductor suppliers engineering test into some of the world's most complicated designs.

About the Speaker:

Janet Olson is Vice President Research and Development for Front-End Design at Cadence Design Systems. Janet is responsible for Modus, Cadence's IC test solution, high level synthesis (Stratus) and constraint verification (Litmus). Janet has a master's degree in Electrical Engineering from Stanford and a bachelor's degree from CMU and holds 7 US patents. Janet has been recognized with the 2017 Marie R. Pistilli Electronic Design Award and the 2016 YWCA Tribute to Women award.

Sessions (Sept. 13)

Date: Sept. 13, Wednesday
Time: 1:00 pm – 2:15 pm

Suffix 's': short presentation

Regular 1A: Hardware Security

Location: Int'l Conf. Hall
Chair: Jiun-Lang Huang (National Taiwan Univ.)

[1A-1] A Physically Unclonable Function Using Time-to-Digital Converter with Linearity Self-Calibration and its FPGA Implementation
Kentaroh Katoh (Fukuoka University), Shuhei Yamamoto, Zheming Zhao, Yujie Zhao, Shogo Katayama, Anna Kuwana, Takayuki Nakatani, Kazumi Hatayama, Haruo Kobayashi (Gunma University), Keno Sato, Takashi Ishida, Toshiyuki Okamoto and Tamotsu Ichikawa (ROHM Semiconductor)

[1A-2] Hunting for Hardware Trojan in Gate Netlist: A Stacking Ensemble Learning Perspective
Liang Hong, Ge Zhu (Northwestern Polytechnical University), Jing Zhou (Beijing Microelectronics Technology Institute), Xuefei Li, Ziyi Chen and Wei Hu (Northwestern Polytechnical University)

[1A-3s] Optimizing Post-Silicon Validation for FPGA Serial Configuration using an Automation Framework and Timing Characterization Verification
Mohd Amiruddin Zainol, Khamron Sompon and Gua Bin Ng (Intel Corporation)

Special 1B: 3D Chiplet Test Session 1

summaries

Location: Room 501
Chair: Xiaoqing Wen (Kyushu Institute of Technology)

[1B-1] On-Chip Timing Circuits for Finding Who's Accountable When a 3D Chiplet IC Fails
Shi-Yu Huang (National Tsing Hua University)

[1B-2] Generating Test Patterns for Chiplet Interconnects: Achieving Optimal Effectiveness and Efficiency
Po-Yao Chuang (imec)

Sessions (Sept. 13)

Special 1C: Siemens Session (Silicon Lifecycle Management)

summaries

Location: Room 601
Chair: Wu Yang (Siemens EDA)

[1C-1] Silent Data Corruption (SDC) Failures — What Do We Know about the Root Causes?
Phil Nigh (Broadcom, Inc.)

[1C-2] Production Test Impacts of Chiplet Integration within a 3DIC
Vineet Pancholi (Amkor Technology, Inc.)

[1C-3] Functional Monitoring of Complex Chips
Lee Harrison (Siemens EDA)

[1C-4] High Protocol Scan with System Level Test
John Jackson (Teradyne, Inc.)

Date: Sept. 13, Wednesday
Time: 2:45 pm – 4:00 pm

Suffix 's': short presentation

Regular 2A: Defect Analysis

Location: Int'l Conf. Hall
Chair: Andre Ivanov (The Univ. of British Columbia)

[2A-1] Toward Improvement and Evaluation of Reconstruction Capability of CapsNet-Based Wafer Map Defect Pattern Classifier
Yuki Yamanaka (Tokyo Metropolitan University), Masayuki Arai (Nihon University), Yoshikazu Nagamura and Satoshi Fukumoto (Tokyo Metropolitan University)

[2A-2] Parametric Faults in Computing-in-Memory Applications of a 4kb Read-Decoupled 8T SRAM Array in 40nm CMOS
Hao-Chiao Hong, Chien-Hung Chen and Yu-Wun Chen (National Yang Ming Chiao Tung University)

[2A-3s] Trustworthy Lifetime Prediction by Aging History Analysis and Multi-Level Stress Test
Chen-Lin Tsai and Shi-Yu Huang (National Tsing Hua University)

Sessions (Sept. 13)

Special 2B: 3D Chiplet Test Session 2

summaries

Location: Room 501
Chair: Senling Wang (Ehime University)

[2B-1] Emerging Trends, Challenges and Solutions for Probing Next Generation Advanced Packaging Devices
Cameron Harker (FormFactor Inc.)

[2B-2] On the application of boundary scan design with embedded time-to-digital converter to 3D stacked IC
Hiroyuki Yotsuyanagi (Tokushima University)

[2B-3] TSV Bonding Evaluation Technology in 3D-IC by Improved Analog Boundary Scan
Shuichi Kameyama (Ehime University)

Special 2C: Industry Session 1

summaries

Location: Room 601
Chair: Jun Matsushima (Renesas Electronics)

[2C-1] Development and Verification of Wet Testing Platform for BioMEMS Chips
Poting Lai (King Yuan Electronics Co., Ltd)

[2C-2] On Evaluation of Technique for Aging Detection and Prediction with Accelerated Life Test
Takaaki Kato (PRIVATECH Inc.)

[2C-3] Innovus Test Points – Enabling the Next Leap in Coverage and Test Pattern Reduction
Janet Olson (Cadence Design Systems, Inc.)

Sessions (Sept. 14)

Date: Sept. 14, Thursday
Time: 1:00 pm – 2:15 pm

Suffix 's': short presentation

Regular 3A: Processor/Software Testing

Location: Int'l Conf. Hall
Chair: Jin-Fu Li (National Central University)

[3A-1] BDD-Based Self-Test Program Generation for Processor Cores
Hao Chen, Chi-Jhe Li, Hung-Lin Chen and Jiun-Lang Huang (National Taiwan University)

[3A-2s] Structured DFT Development Approach for Chisel-Based High Performance RISC-V Processors
Bin Zhang, Ye Cai (ShenZhen University), Zhiheng He (Beijing Institute of open source chip), Sen Liang (Chinese Academy of Sciences) and Wei He (PengCheng Laboratory)

[3A-3s] Software Defect Detection Based on Feature Fusion and Alias Analysis
Xuejian Li and Zhengguang Zhu (Anhui University)

Regular 3B: Fault Tolerant Latch

Location: Room 501
Chair: Tong-Yu Hsieh (National Sun Yat-sen Univ.)

[3B-1] A Low Overhead and Double-Node-Upset Self-Recoverable Latch
Aibin Yan, Fan Xia (Anhui University), Tianming Ni (Anhui Polytechnic University), Jie Cui (Anhui University), Zhengfeng Huang (Hefei University of Technology), Patrick Girard (University of Montpellier) and Xiaoqing Wen (Kyushu Institute of Technology)

[3B-2] Design of a Novel Latch with Quadruple-Node-Upset Recovery for Harsh Radiation Hardness
Aibin Yan, Chao Zhou, Shaojie Wei, Jie Cui (Anhui University), Zhengfeng Huang (Hefei University of Technology), Patrick Girard (University of Montpellier) and Xiaoqing Wen (Kyushu Institute of Technology)

[3B-3] Design of Single Node Upset Resilient Latch for Low Power, Low Cost and Highly Robust Applications
Anwesh Kumar Samal, Sandeep Kumar and Atin Mukherjee (National Institute of Technology Rourkela)

Sessions (Sept. 14)

summaries

Special 3C: Industry Session 2

Location: Room 601
Chair: Kazumi Hatayama (EVALUTO)

[3C-1] Strategies to Reduce Memory Test Time during Power-On Self-Test for Automotive Products
Yudai Kawano (Renesas Electronics Corporation)

[3C-2] mm-Wave Connection Technology for Semiconductor Test
Hiroyuki Yamakoshi (S.E.R. Corporation)

[3C-3] High Accuracy Defect Identification Method by using TDR with Femto-second Laser Technology
Makoto Shinohara (ADVANTEST CORPORATION)

Date: Sept. 14, Thursday
Time: 2:45 pm – 4:00 pm

Suffix 's': short presentation

Regular 4A: Testing and Verification

Location: Int'l Conf. Hall
Chair: Yoshinobu Higami (Ehime University)

[4A-1] On Test Pattern Generation Method for an Approximate Multiplier Considering Acceptable Faults
Shogo Tokai, Daichi Akamatsu, Hiroyuki Yotsuyanagi and Masaki Hashizume (Tokushima University)

[4A-2s] Feasibility Study of Incremental Neural Network Based Test Escape Detection by Introducing Transfer Learning Technique
Ayano Takaya and Michihiro Shintani (Kyoto Institute of Technology)

Regular 4B: Memory

Location: Room 501
Chair: Hao-Chiao Hong (National Yang Ming Chiao Tung University)

[4B-1] Integrated Progressive Built-In Self-Repair (IPBISR) Techniques for NAND Flash Memory
Shyue-Kung Lu and Xin Dong (National Taiwan University of Science and Technology)

[4B-2] Design of A Highly Reliable and Low-Power SRAM With Double-Node Upset Recovery for Safety-critical Applications
Aibin Yan, Jing Xiang (Anhui University), Zhengfeng Huang (Hefei University of Technology), Tianming Ni (Anhui Polytechnic University), Jie Cui (Anhui University), Patrick Girard (University of Montpellier) and Xiaoqing Wen (Kyushu Institute of Technology)

[4B-3] Fault-Aware ECC Scheme for Enhancing the Read Reliability of STT-MRAMs
Meng-Shan Wu, Yen-Lin Chua, Jin-Fu Li (National Central University), Yun-Ting Chuan and Shih-Hsu Huang (Chung Yuan Christian University)

Regular 4C: Jitter and Error Mitigation

Location: Room 601
Chair: Haruo Kobayashi (Gunma University)

[4C-1] Experimental Evaluation of Jitter Reduction Methods for Multi-Gigahertz Test
David Keezer (Georgia Institute of Technology), Dany Minier (Boreas Technologies) and Hongjie Li (Shenzhen Research Institute Tianjin University)

[4C-2s] Self-Sufficient Clock Jitter Measurement Methodology Using Dithering-Based Calibration
Yi-Hsuan Lee, Wei-Hao Chen and Shi-Yu Huang (NTHU)

[4C-3s] Cost-Effective Error-Mitigation for High Memory Error Rate of DNN: A Case Study on YOLOv4
Wei-Ji Chao and Tong-Yu Hsieh (National Sun Yat-sen University)

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